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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/730,609	12/08/2003	Feng Dan Lin	DB001099-000	4033

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EXAMINER	
NGUYEN, LINH M	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 07/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/730,609	LIN, FENG DAN	
	Examiner	Art Unit	
	Linh M. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14-35* is/are allowed.

6)☒ Claim(s) *1,2,4,6,7 and 36* is/are rejected.

7)☒ Claim(s) *3,5 and 8-13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-36 are presented in the instant application according to the Applicant's amendment filing on 05/23/2005.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2, 4, 6-7 and 36 are rejected under 35 U.S.C. 102(b) as being anticipated by Hamamoto et al. (U.S. Patent No. 6,417,715).

With respect to claim 1, Hamamoto et al. discloses, in Fig. 3, a method of operating a synchronous circuit comprising a) obtaining a reference clock [EXT.CLK] and an inverted reference clock [EXT./CLK] for the synchronous circuit; b) using a delay line [130] as part of the synchronous circuit to generate a feedback clock [CLK2]; and c) selectively [125] using one of the reference clock and the inverted reference clock as an input to the delay line based on a relationship among the phases of the reference clock, the inverted reference clock, and the feedback clock.

With respect to claim 2, Hamamoto et al. further discloses, in Fig. 3, obtaining a delayed feedback clock by delaying the feedback clock by a predetermined time delay [140].

With respect to claim 4, Hamamoto et al. further discloses, in Fig. 3, using the delayed feedback clock to determine the relationship among the phases of the reference clock, the inverted reference clock, and the feedback clock.

With respect to claim 6, Hamamoto et al. discloses, in Fig. 3, a method of operating a synchronous circuit comprising a) obtaining a reference clock [EXT.CLK] and an inverted reference clock [EXT./CLK] for the synchronous circuit; b) using a delay line [130] as part of the synchronous circuit to generate a feedback clock [CLK2]; c) obtaining a delayed feedback clock [RCLK] from the feedback clock; and d) selectively [125] using one of the reference clock and the inverted reference clock as an input to the delay line based on a relationship among the phases of the reference clock, the inverted reference clock, the feedback clock and the delayed feedback clock.

With respect to claim 7, Hamamoto et al. discloses, in Fig. 3, that obtaining the delayed feedback clock includes delaying [140] the feedback clock by a predetermined time delay to obtain the delayed feedback clock.

With respect to claim 36, Hamamoto et al. discloses, in Fig. 3, a method of operating a synchronous circuit comprising a) obtaining a reference clock [EXT.CLK] and an inverted reference clock [EXT./CLK] for the synchronous circuit; b) using a delay line [130] as part of the synchronous circuit to generate a feedback clock [CLK2]; c) obtaining a delayed feedback clock [RCLK] from the feedback clock; and d) selectively [125] using one of the reference clock and the inverted reference clock as an input to the delay line based on a relationship among the phases of the reference clock, the inverted reference clock, and one of the feedback clock and the delayed feedback clock.

Allowable Subject Matter

3. Claims 14-35 are allowed.

4. Claims 3, 5 and 8-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is a statement of reasons for the indication of allowable subject matter:

The closest prior art of record does not show or fairly suggest:

a) A method of operating a synchronous circuit, in which the selectively using step includes sampling the reference clock and the inverted reference clock using the feedback clock to obtain a first logic value and a second logic value respectively; further sampling the reference clock and the inverted reference clock using the delayed feedback clock to obtain a third logic value and a fourth logic value respectively; using the inverted reference clock as an input to the delay line so long as the fourth logic value is "0" and the third logic value is "1" along with a value of "1" for one of the first and the second logic values, as called for in claim 3;

b) A method of operating a synchronous circuit, in which the step of selectively using includes sampling the reference clock and the inverted reference clock using the delayed feedback clock to obtain a first logic value and a second logic value respectively; and using the inverted reference clock as the input to the delay line so long as the first logic value is "1" and the second logic value is "0", as called for in claim 5;

c) A method of operating a synchronous circuit, which includes a step of adjusting a predetermined time delay based on at least one of the following: how far away a lock point of the synchronous circuit establishing a lock between a reference clock and a feedback clock can be

moved from an initial entry point; frequency of the feedback clock; and a tuning range of the synchronous circuit after establishing the lock between the reference clock and the feedback clock, as called for in claim 8;

d) A method of operating a synchronous circuit, in which the step of selectively using includes: obtaining a first phase relationship between the feedback clock and the reference clock; obtaining a second phase relationship between the feedback clock and the inverted reference clock; obtaining a third phase relationship between the delayed feedback clock and the reference clock; obtaining a fourth phase relationship between the delayed feedback clock and the inverted reference clock; and using the inverted reference clock as the input to the delay line based on the first, the second, the third, and the fourth phase relationships, as called for in claim 9;

e) A method of a synchronous circuit, in which the step of selectively using includes: sampling the reference clock and the inverted reference clock using the feedback clock to obtain a first logic value and a second logic value respectively; further sampling the reference clock and the inverted reference clock using the delayed feedback clock to obtain a third logic value and a fourth logic value respectively; using the inverted reference clock as the input to the delay line so long as the fourth logic value is "0" and the third logic value is "1" along with a value of "1" for one of the first and the second logic values, as called in claim 12;

f) A method of a synchronous circuit, in which the step of selectively using includes: sampling the reference clock and the inverted reference clock using the delayed feedback clock to obtain a first logic value and a second logic value respectively; using the inverted reference clock as an input to the delay line so long as the first logic value is "1" and the second logic value is "0", as called for in claim13;

g) A method of operating a synchronous circuit including a step of selectively using one of a reference clock and an inverted reference clock as an input to a delay line based on individual sampling of the reference clock and the inverted reference clock with each of a feedback clock and a delayed feedback clock, as called for in independent claim 14;

h) A synchronous circuit including a decoder circuit coupled to a delay line and configured to receive a feedback clock as a first input and to generate a delayed feedback clock therefrom, in which the decoder circuit is further configured to receive a reference clock as a second input and an inverted reference clock as a third input, the decoder circuit is configured to determine a relationship among the phases of the reference clock, the inverted reference clock, the feedback clock, and the delayed feedback clock, and to selectively supply one of the reference clock and the inverted reference clock as the input clock to the delay line based on determination of the phase relationship, as called for in independent claim 19;

i) A synchronous circuit including a decoder circuit coupled to a delay line and configured to receive a feedback clock as a first input and to generate a delayed feedback clock therefrom, in which the decoder circuit is further configured to receive a reference clock as a second input and an inverted reference clock as a third input, the decoder circuit is configured to determine a relationship among the phases of the reference clock, the inverted reference clock, and at least one of the feedback clock and the delayed feedback clock, and to selectively supply one of the reference clock and the inverted reference clock as the input clock to the delay line based on determination of the phase relationship, as called for in independent claim 28;

j) A synchronous circuit including a decoder circuit coupled to a delay line and configured to receive a feedback clock as a first input and to generate a delayed feedback clock

therefrom, in which the decoder circuit is further configured to receive a reference clock as a second input and an inverted reference clock as a third input, the decoder circuit is configured to determine a relationship among the phases of the reference clock, the inverted reference clock, and the delayed feedback clock, and to selectively supply one of the reference clock and the inverted reference clock as the input clock to the delay line based on determination of the phase relationship, as called for in independent claim 29;

k) A synchronous circuit including a decoder circuit coupled to a delay line and configured to receive a feedback clock as a first input and to generate a delayed feedback clock therefrom, in which the decoder circuit is further configured to receive a reference clock as a second input and an inverted reference clock as a third input, the decoder circuit is configured to determine a relationship among the phases of the reference clock, the inverted reference clock, and at least one of the feedback clock and the delayed feedback clock, and to selectively supply one of the reference clock and the inverted reference clock as the input clock to the delay line based on determination of the phase relationship, as called for in independent claim 30; and

l) A method of operating a synchronous circuit including a step of selectively using one of a reference clock and an inverted reference clock as an input to a delay line based on individual sampling of the reference clock and the inverted reference clock with the delayed feedback clock, as called for in claim 31.

Remarks

6. Claims 1-2, 4, 6-7 and 36 are now being rejected based on newly found prior art to Hamamoto et al. as set forth in the office action.

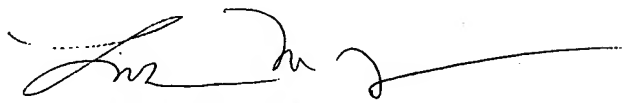
Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LMN



LINH MY NGUYEN
PRIMARY EXAMINER